Abstract of the Disclosure

A network switch port includes a cell memory, a queuing system, a data path controller and an output buffer. The data path controller stores incoming cells derived from network data transmissions in the cell memory. The queuing system generates the cell memory address of each stored cell when the cell is to be forwarded from the cell memory, and the data path controller appends the cell memory address of that cell to a linked list of addresses of cells to be forwarded from the memory. When the linked list is not empty, the data path controller forwards cells from the cell memory to the output buffer in the order that their cell memory addresses were appended to the linked list. The output buffer stores and then sequentially forwards the cells outward from the switch port to a receiving network component which store them in a cell buffer until it can forward them elsewhere. The receiving network component produces a multiple- bit back pressure data indicating how much of its cell buffer is currently filled with cells. Depending on the fill amount the back pressure data indicates, the output buffer either halts or continues to forward cells to the receiving network component, and either halts or continues allowing the data path controller to forward cells from the cell memory to the output buffer.